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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DEBORAH T. MARR

Appeal 2008-006289
Application 09/490,172
Technology Center 2100

Before: ST. JOHN COURTNENAY, III, THU A. DANG, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

STEPHENS, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

Appellant appeals under 35 U.S.C. § 134(a) (2002) from a final rejection of claims 1, 3-11, and 13-21. Claims 2 and 12 have been canceled. (App. Br., 2; Claims App.x 9, 11). We have jurisdiction under 35 U.S.C. § 6(b) (2008).

We AFFIRM.

Introduction

According to Appellant, the invention is a system and method for a multi-threaded processor (Abstract). One or more variables are set up in memory indicating the priority level of a plurality of executable threads (*id.*). Instructions having a higher priority thread may be executed more than those with a lower priority thread or may be given comparatively more access to resources such as memory or buses (*id.*).

STATEMENT OF THE CASE

Exemplary Claim(s)

Claim 1 is an exemplary claim and is reproduced below:

1. A method comprising:

> assigning a value in memory to indicate which of a plurality of threads executed by a single processor has a higher priority;
>
> allocating a resource between said plurality of threads depending on a priority assigned to each thread; and
>
> providing a counter with a predetermined value for said plurality of threads, said value being selected by control logic depending on the priority assigned to each thread, said counter

being used in said allocating operation.

Prior Art

Olarig	5,944,809	Aug. 31, 1999
Kimura	6,105,127	Aug. 15, 2000

Rejections

Claims 1, 3-11, and 13-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura and Olarig.

GROUPING OF CLAIMS

Appellant argues all the independent claims, claims 1, 10, 11, and 20, as a group on the basis of claim 1 (App. Br. 5-7). We select independent claim 1 as the representative claim. Since none of the dependent claims 3-9, 13-19, and 21 have been argued separately, they stand or fall with representative claim 1.

We accept Appellant's grouping of the claims. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

Appellant asserts that her invention is not obvious over Kimura and Olarig because Olarig fails to teach "a counter with a predetermined value for said plurality of threads, said value being selected by control logic depending on the priority assigned to each thread, said counter being used in said allocating operation" (App. Br. 5-7). Specifically, Appellant contends Olarig is directed toward balancing workload for interrupts among several

processors – not one processor – and does not provide control logic selecting the predetermined value based on the threads' priorities (App. Br. 7). Thus, according to Appellant, Olarig teaches a system with multiple processors and a counter that sets up values to identify the processing unit (Reply 3-4.).

The Examiner finds Olarig discloses an integrated MP-compatible interrupt controller schema that controls or balances system resource allocation to a bus agent based on a "rotating priority" arbitration protocol controlled by Local/Central Programmable Interrupt Controllers (Ans. 8). Thus, according to the Examiner, one of ordinary skill in the art at the time the invention was made would have looked to incorporate this feature into the system of Kimura to determine the overall priority level of a processor resulting in an upgraded advanced multi-processor, multi-thread system that provides a cost-effective solution and dynamically balances allocation or delivery of system resources based on the total task priority derived from the "rotating priority" arbitration logic control (Ans. 8-9).

Issue 1: Has Appellant shown the Examiner erred in finding the combination of Kimura and Olarig would have taught or suggested a counter with a predetermined value for threads such that the value is selected by control logic depending on the priority assigned to each thread and the counter is used in the allocating operation? (*See* Claim 1).

FINDINGS OF FACT (FF)

Kimura

(1) Kimura teaches a multithread processor for executing multiple instruction streams (Abstract). The processor includes a holding unit for holding the priority level of each of the instruction streams; and a control unit that decides which decoded instruction should be issued to a function unit designated by two or more instruction issue requests at the same time, in accordance with the priority levels held by the holding unit (Abstract).

(2) The instruction to be issued to each functional unit (or the decode result of the instruction) is determined in accordance with priority levels. The priority level of the instruction stream to which the instruction belongs is set by one functional unit. Therefore, the variation of load among the multiple instruction streams can be flexibly adjusted in accordance with the priority levels. As a result, the execution of each instruction stream can be achieved efficiently so as to improve the overall throughput of the processor. (Col. 3, ll. 13-20, col. 8, ll. 34-58, col. 9, ll. 61-63, and Fig. 4).

Olarig

(3) Olarig teaches a method and system directed toward distributing interrupts in a multiprocessor system (col. 1, ll. 20-22).

(4) A centralized interrupt controller, between a host bus and system bus, receives interrupts from their sources and routes them to their destinations. A counter having a two bit-length, is provided with each processing unit and appended to that processing unit's task priority register (4 –bits). This task priority register along with the appended counter

determine the overall priority level for that processing unit. (Col. 3, ll. 18-35).

(5) The system provides a cost-effect solution with an MP-compatible interrupt controller scheme that "guarantees balanced delivery of interrupts to a processor that has the lowest current task priority among two or more processors" (col. 4, ll. 7-11).

(6) In an example, each of four processors is provided with a two-bit counter initialized to either 00, 01, 10, or 11. Each of these two-bit counters is appended to a four-bit task priority register associated with a processor essentially giving each a six-bit internal priority level. Therefore, even if all four-bit task priority registers contain the same priority data, each of the four processors will have a different six-bit internal priority level. (Col. 6, ll. 42-57).

ANALYSIS

We find that Kimura's instruction streams teach or suggest Appellant's claimed plurality of threads, each having a priority level set by a functional unit (control logic) for executing by a processor (FF 1 and FF2). We also find Olarig teaches a counter with a predetermined value used to determine the task priority and overall priority level for a processing unit (FF 4-5). We further find that Olarig teaches control logic to select the counter value (FF 6).

In light of these findings, we agree with the Examiner that the combination of Kimura's teaching of instruction streams which are assigned a priority level and Olarig's teaching of using a counter with a predetermined value to indicate a priority level would have taught or

suggested Appellant's claimed counter with a predetermined value for threads.

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

See KSR Int'l. Co. v. Teleflex Inc., 127 S.Ct. 1727, 1740 (2007).

To facilitate review, this analysis should be made explicit. But it need not seek out precise teachings directed to the challenged claim's specific subject matter, for a court can consider the inferences and creative steps a person of ordinary skill in the art would employ. *Id.* at 418.

Here we conclude that substituting the counter taught by Olarig into the system of Kimura, which also has a priority level set, to indicate a priority level would have been a predictable variation and a simple substitution within the skill of an ordinary artisan at the time the invention was made. Indeed, the counter of Olarig is a predictable variation of bits used to indicate the priority level and substituting this variation of a priority level indicator into the system of Kimura, which also uses bits to indicate priority level, would have been obvious to a skilled artisan.

Therefore, after considering the arguments and evidence presented, Appellant has failed to persuade us of error in the Examiner's finding that the combination of Kimura and Olarig would have taught or suggested a counter with a predetermined value for threads such that the value is selected by control logic depending on the priority assigned to each thread and the

counter is used in the allocating operation, as recited in claim 1. Claims 3-9, 13-19, and 21, not separately argued, fall with representative claim 1. *See* 37 C.F.R. § 41.37(c)(1)(vii).

DECISION

The Examiner's rejection of claims 1, 3-11, and 13-21 under 35 U.S.C. § 103(a) as being unpatentable over Kimura and Olarig is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2009).

AFFIRMED

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